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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,367	02/28/2002	Ryota Nanjo	020200	9203

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EXAMINER
THOMAS, TONIAE M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/084,367

Applicant(s)

NANJO ET AL.

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 1-9 and 13-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 10-12, 27 and 28 is/are rejected.
- 7) ☒ Claim(s) 25 and 26 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09 February 2004 has been entered.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. *Claims 10, 11, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsai et al. (US 5,668,024).*

The Tsai et al. patent (Tsai) discloses a method of manufacturing a semiconductor device (figs. 1-10 and col. 3, line 45 - col. 6, line 63). The method comprises the following steps, as recited in claim 10: preparing a semiconductor substrate 1 having first and second regions of a first conductivity type, p-type, which are defined by isolation regions 2 in a principal surface area of the substrate (fig. 1 and col. 3, lines 50-

55);<sup>1</sup> forming at least a first gate electrode 12 in a partial area of the first region (fig. 3 and col. 4, lines 31-44);<sup>2</sup> implanting impurities of a second conductivity type opposite to the first conductivity type, n-type, into a surface layer of the second region (fig. 1 and col. 4, lines 8-13), and thereafter executing a first activation process to form a first impurity diffusion region 8 shallower than the isolation regions (col. 4, lines 27-31);<sup>3</sup> forming a first spacer film 14 on the side surface of the first gate electrode (fig. 4 and lines 47-61); by using the first gate electrode and the first spacer film as a mask, implanting impurities of the second conductivity type into a surface layer of the first region (fig. 5 and col. 4, line 67 – col. 5, line 5), and thereafter executing a second activation process to form a second impurity diffusion region 16 (col. 5, lines 12-18); removing the first spacer film (fig. 8); and using the first gate electrode as a mask, implanting impurities of the second conductivity type into a surface layer in the first region (fig. 10 and col. 6, lines 12-17 and lines 26-31), and thereafter executing a third activation process to form third impurity diffusion region 22 (col. 6, lines 60-63). The third activation process is sufficient to cause the gradient of an impurity concentration distribution in a p-n junction formed by the third impurity diffusion region 22 to become steeper than the gradient of an impurity concentration distribution in a p-n

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<sup>1</sup> The first region of the substrate comprises NMOS region 5, and the second region comprises PMOS region 4.

<sup>2</sup> See Appendix A.

<sup>3</sup> Tsai does not explicitly state that the thermal oxidizing process used to form oxide layer 11 is an activation process. However, since the annealing process is performed at a temperature within the range of 800°C - 1000°C, it is inherent that the implanted impurities are activated during the formation of oxide layer 11.

junction formed by the first impurity diffusion region 8, and steeper than the gradient of an impurity concentration distribution of a p-n junction formed by the second impurity diffusion region 16, as recited in claims 10 and 28, respectively.

The first, second, and third activation processes include a thermal treatment at a temperature at least equal to 750°C, as recited in claim 11 (col. 4, lines 27-31; col. 5, lines 12-18; and col. 6, lines 60-63).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. *Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai in view of Shibata (US 4,622,735).*

Tsai lacks anticipation in not teaching that the third activation process is a laser thermal process. Shibata discloses a method for forming an integrated circuit (e.g. figs. 1A-1G and accompanying text). The method comprises implanting impurities, and executing an activation process using a laser thermal process to form impurity diffusion regions (col. 3, lines 21-31).

The third impurity diffusion region 22 is an ultra lightly doped source/drain region (Tsai - fig. 8). It would have been obvious to one of ordinary skill in the art, at

the time the invention was made, to combine Tsai and Shibata, since laser annealing forms source/drain regions with low resistivity.

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai in view of Shibata as applied to claim 12 above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era - Vol. 1: Process Technology).

While Tsai teaches that the second activation process is performed using a rapid thermal annealing process (col. 4, lines 27-31), Tsai does not teach that the first activation process is executed using a rapid thermal annealing process.

As discussed previously, the first activation process occurs during the formation of thermal oxide layer 11. The Wolf et al. reference (Wolf) teaches using a rapid thermal annealing process to form thermal oxide (page 58 - par. 3, lines 3-6):

During rapid thermal annealing, the substrate is subjected to high temperatures long enough to achieve the desired process effect, but with minimum dopant diffusion (Wolf page 57 - par 3, lines 2-3). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Tsai and Shibata, by executing the first activation process using a rapid thermal annealing process, as taught by Wolf, since rapid thermal annealing subjects the substrate to high temperatures long enough to grow a thermal oxide layer with minimum dopant diffusion in the well regions 7, 10b and threshold voltage regions 8, 10a.

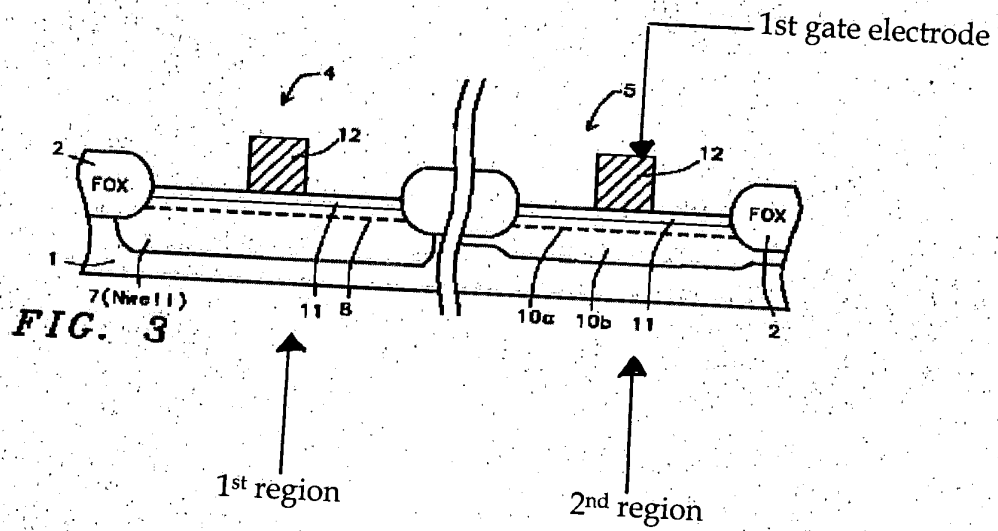
***Allowable Subject Matter***

5. *Claims 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.* The prior art of record does not anticipate, teach, or suggest a method of manufacturing a semiconductor device comprising the steps substantially as claimed, wherein impurities of a second conductivity type - opposite the first conductivity type - are implanted into a surface layer of the second region to form a first impurity diffusion region, the first impurity region forming a resistor.

***Response to Arguments***

6. Applicant's arguments with respect to claim 10 have been considered but are moot in view of the new ground(s) of rejection.

Appendix



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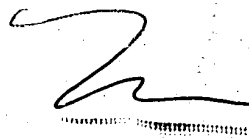
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ

10 May 2004



**Mary Wilczewski**  
**Primary Examiner**